REMARKS

This is a response to the Office Action dated August 3, 2005. Claims 1-41 are pending in the application. In the Office Action, Claims 1-5, 8-9, 11-15, 18-19, 21-28, 31, 33-36, 39, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,313,586 to Serge Rutman ("Rutman") in view of European Patent Application EP 1061439A1 to Andrea Olgiati ("Olgiati"). Claims 6-7, 16-17, 29-30, and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Olgiati and further in view of U.S. Patent No. 5,870,109 to Joel C. McCormack et al. ("McCormack et al."). Claims 10, 20, 32, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Olgiati and further in view of Betty Prince, "High Performance Memories," 1996 ("Prince").

The rejections from the Office Action of August 3, 2005 are discussed below in connection with the various claims. No new matter has been added. Reconsideration of the application is respectfully requested in light of the following remarks.

I. REJECTIONS UNDER 35 U.S.C. § 103(a)

A. REJECTIONS UNDER RUTMAN IN VIEW OF OLGIATI

Independent claims 1, 11, 24, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Olgiati. Applicants submit that claims 1, 11, 24 and 34 are patentable over Rutman in view of Olgiati because the combination of Rutman and Olgiati fails to disclose all of the elements of these claims.

Independent claim 1 relates to a "packet processing system." The system includes: "a processor; a co-processor separated from said processor by a boundary; and an interface coupled with said processor and said co-processor and operative to bridge said boundary , said interface including: a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said

memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 11 relates to an "interface for coupling a processor to a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The interface includes: "a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor ; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously"

Independent claim 24 relates to a "method of interfacing a processor with a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The method includes: "(a) receiving first data from said processor via a first interface; (b) storing said first data in a memory; (c) signaling said co-processor that said first data has been stored; (d) receiving a read command from said co-processor via a second interface; and (e) providing said first data to said co-processor via said second interface across said boundary ; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 34 relates to an "apparatus for facilitating communications between a first processor and a second processor." The apparatus includes: "a dual port memory coupled with said first processor via first interface and said second processors via a second interface, and operative to act as a message buffer between said first processor and said second processor; control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors of

said communications; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Rutman discloses, "A special type of random access memory referred to as video random access memory (VRAM) is used through to provide multiple access to the memory in a timely manner. The VRAM is characterized by a random access port which enables random accessing to the memory array and a serial port comprising a shift register for outputting a large group of bits of data, such as pixels representative of a scan line of a video image, which are rapidly output by the memory. In the present invention, the VRAM is utilized in a different manner to provide more efficient use of memory without degradation in system performance. The VRAM provides for communications between processors as well as the memory utilized by the coprocessor for storage of code and data. Communications between processors is performed through the serial port; therefore, data is communicated via blocks of data transfers minimizing the frequency of access to the memory array. The co-processor, which utilizes the memory for processing and code storage, communicates with the memory through the random access port in order for the co-processor to perform its functions in a timely manner. The co-processor will only be interrupted in its access of the memory when it is determined that blocks of data are to be transferred into the or out of the memory via the serial port." *See* Rutman, Abstract.

Olgiati discloses, "A computer system .... which comprises a first processor 1, a second processor 2 for use as a coprocessor to the first processor 1 and a memory 3. There are also provided data buffers 5 for buffering data to be written to, or read from, the memory 3 in data bursts in accordance with burst instructions. These burst instructions are executed by a burst controller 7, and are provided in sequence for execution by a burst instruction queue 6. Burst instructions are provided by the first processor 1 to the burst instructions queue 6, and data is read from, and written to, the memory 3 by the second processor 2 through the data buffers 5 in accordance with burst instructions executed by the burst controller 7. Coprocessor instructions are provided to control execution of the coprocessor 2, and synchronisation between coprocessor instructions and burst instructions is achieved by a synchronisation mechanism 10, 11 and use of specific coprocessor and burst instructions." *See* Olgiati, Abstract.

As noted in the Office Action, Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as required by claims 1, 11, 24, and 34.

Olgiati fails to fill the gap. Instead, the system of Olgiati includes a main processor, a coprocessor, a main memory, a burst buffer memory, a cache, a burst instruction queue, and a coprocessor instruction queue. *See* Olgiati, Fig. 1. This configuration differs from Applicants' claimed methods and systems in many respects.

First, interprocessor communication in Olgiati is performed via instruction queues, not via a shared memory. The main processor of Olgiati communicates with the coprocessor by providing instructions for particular tasks through the burst instruction queue (for tasks such as configuration of the burst buffer controller; and transfer of data between the burst buffer memory and the main memory) or the coprocessor instruction queue (for tasks such as overall control of the coprocessor). In contrast, Applicants' claim systems and methods that use a shared memory for inter-processor communication.

Second, the Olgiati processor has access to a fast access memory cache 4 implemented in SRAM in a conventional manner, but not the main memory implemented in DRAM. The coprocessor, on the other hand, receives and stores data through interaction with the burst buffers implemented in SRAM, which in turn interface with main memory (DRAM) in accordance with the burst instructions. In other words, the processor and coprocessor of Olgiati interact via a host of different memories. Indeed, the use of the instruction queues decouples the execution of processor 1 from the execution of the burst buffer memory, the only memory accessible to the coprocessor. As such, Olgiati fails to describe a system in which a processor and coprocessor may access a shared memory independently as claimed, much less a system in which such independent access may be performed substantially simultaneously. Even assuming arguendo that the Olgiati processor could access the SRAM cache while the coprocessor accesses the SRAM burst memory (a point on which Olgiati is silent), these processors are accessing different memories, not a shared memory as claimed.

For at least these reasons, Olgiati fails to disclose a system, "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Even assuming that Olgiati filled the gap left by Rutman, there is no motivation to combine these mutually exclusive architectures. As described above, Olgiati discloses a system that uses many different memories and mechanisms to maximize the efficiency of a coprocessor. Rutman, on the other hand, is concerned with extracting maximum efficiency from a single memory. For example, Rutman notes, "To save on space and achieve the greatest memory

utilization, a single memory such as a dynamic random access memory (DRAM) is used to provide memory for storage of code and data utilized by the co-processor to perform its tasks." Pointing out the benefits of his system, Rutman later notes, "The resultant effect is the use of a single memory to save on chip space and the minimization of memory access by the main processor for communications thereby freeing the same memory for frequent access by the slave processor for code and data." One of ordinary skill in the art would appreciate that the primary benefits of increased efficiency while the minimizing space and costs associated with additional memories described in Rutman would be eviscerated by adding these additional memories and instruction queues to incorporate the system of Olgiati.

For at least these reasons, claims 1, 11, 24, and 34, as amended, are patentable over Rutman in view of Olgiati. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

Dependent claims 2-5, 8-9, 12-15, 18-19, 21-23, 25-28, 31, 33, 35-36, 39, and 41 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Olgiati. Dependent claims 2-5, 8-9, 12-15, 18-19, 22-23, 25-28, 31, 35-36, and 39 should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

B. REJECTIONS OVER RUTMAN IN VIEW OF OLGIATI AND FURTHER IN VIEW OF MCCORMACK ET AL.

Dependent claims 6-7, 16-17, 29-30, and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of McCormack. Applicants submit that claims 6-7, 16, 17, 29, 30 and 37-38 are patentable over Rutman in view of McCormack because these references, alone or in combination, fail to teach or suggest all of the elements of these claims.

The combination of Rutman and Olgiati is described above.

McCormack discloses, "A graphics system for storing and editing graphic images represented by digital data, includes a frame memory for storing pixel data representing graphic images including first and second graphic objects. The pixel data is stored at addresses, each being associated with one or more graphic fragment forming the first and second graphic objects. First and second addresses are respectively associated with those of the graphic fragments forming the first and second graphic objects. A memory controller controls writing and reading the pixel data to and from the frame memory. A fragment editor is provided to receive the pixel

data read from the first address and modify the associated fragment with the received pixel data so as to form modified pixel data. An address detector detects the first address responsive to a request to read the pixel data from the first address and the second address responsive to a subsequent request to read pixel data from the second address. The detector compares the detected first and second addresses to identify an overlap of the first and second graphic objects. If an overlap is identified, the controller controls the writing of the modified pixel data to the first address before the reading of the pixel data from the second address."

As described above with respect to the rejections under 35 U.S.C. § 103(a), Rutman and Olgiati at least fail to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously." McCormack et al. fails to fill the gap. McCormack discloses a graphic system which detects overlap between multiple graphic objects to ensure that each frame in the overlap is rendered properly. Nowhere does McCormack et al. disclose or suggest a system "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as claimed.

For at least these reasons, claims 6-7, 16-17, 29-30, and 37-38 are patentable over Rutman in view of Olgiati and further in view of McCormack et al. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

C. REJECTIONS OVER RUTMAN AND OLGIATI IN VIEW OF PRINCE

Claims 10, 20, 32, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Olgiati and further in view of Prince. Applicants submit that claims 10, 20, 32 and 40 are patentable over Rutman in view of Olgiati and further in view of Prince because these references, alone or in combination, fail to teach or suggest all of the elements of these claims.

The combination of Rutman in view of Olgiati is described above.

Prince generally describes the advantages of Synchronous RAM, such as burst synchronous SSRAMs, and includes statistics on the number of cycles required for first through fourth memory accesses.

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously." Prince fails to fill the gap. Prince merely discloses the benefits of using various types of synchronous RAMs. Nowhere does Prince disclose or

suggest a system "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as claimed.

For at least these reasons, claims 10, 20, 32, and 40 are patentable over Rutman in view of Prince. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

SUMMARY

Each of the rejections in the Office Action dated August 3, 2005 has been addressed and no new matter has been added. Applicants submit that all of the pending claims are in condition for allowance and notice to this effect is respectfully requested. The Examiner is invited to call the undersigned if it would expedite the prosecution of this application.

Respectfully submitted,

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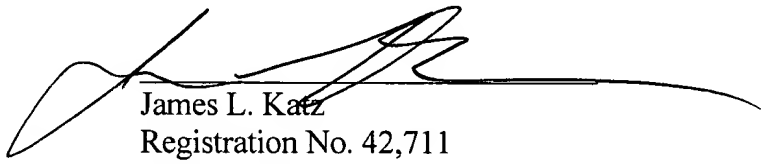

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